

# FSSR2, a Self-Triggered Low Noise Readout Chip for Silicon Strip Detectors

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**Abstract**— The FSSR2 is the second release of the Fermilab Silicon Strip Readout Chip. The chip has been designed and fabricated in a 0.25  $\mu\text{m}$  CMOS technology for high radiation tolerance. The first release, simply called the FSSR, was a prototype version with many different analog front-end configurations. The best solution was chosen for the FSSR2 chip to optimize the noise, according to criteria discussed in this paper. The FSSR2 has been designed for the silicon strip detectors of the BTeV experiment. The chip services 128 strips and provides address, time and magnitude information for all hits. Several programmable features are included in FSSR2, such as an internal pulser, a baseline restorer and a signal peaking time selectable among four values in the range between 65 ns and 125 ns. The circuit design and the performances of FSSR2 are discussed in this paper.

**Index Terms** —Front-end electronics, CMOS, Noise, silicon strip detectors

## I. INTRODUCTION

A FULL custom integrated circuit called the FSSR2 (Fermilab Silicon Strip Readout) chip has been designed and fabricated in the TSMC (Taiwan Semiconductor Manufacturing Company) 0.25  $\mu\text{m}$  CMOS process to interface with silicon strip detectors and send digital information to the data acquisition system.

FSSR2 is the final step of an R&D effort which began with the design of the prototype chip FSSR [1]. The architecture of both FSSR and FSSR2 is a modified version of that of the FPIX2, the readout chip for the BTeV pixel detector [2]. FSSR2 has 128 analog channels, each consisting of a charge-sensitive preamplifier, a unipolar semigaussian shaper, a selectable baseline restorer (BLR), a hit discriminator and a 3-bit Flash analog-to-digital converter (ADC). The chip operates in a self-triggered mode with no analog storage.

The chip was designed for the readout of the Forward Silicon Tracker of the BTeV experiment at Fermilab. However, as discussed in the following, the performances of

FSSR2 make it suitable for a wide range of applications with microstrip detectors. Fig. 1 is a photo of the FSSR2 chip.

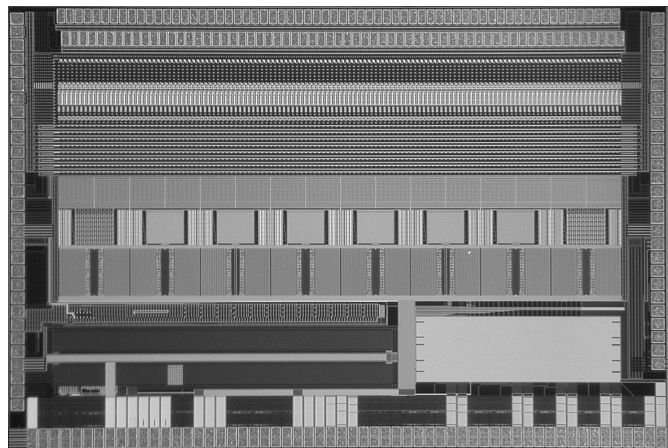


Fig. 1. Photograph of the FSSR2 chip with input pads at the top. The chip measures 7.5 mm x 5 mm and the input pads have an effective pitch of 50  $\mu\text{m}$ .

## II. CHIP DESCRIPTION

### A. Chip Specifications and FSSR2 Architecture

The FSSR2 chip can be considered as comprised of several parts, as shown in Fig. 2. The chip core consists of 128 analog channels, logically subdivided in 16 sets of 8 analog channels each, of the end-of-set logic (16 blocks, one for each set of front-end channels) and of the core logic, which controls the data flow from the core to the data output interface. If a hit is detected in one of the channels, the core transmits a 24-bit data word which carries information relevant to pulse amplitude, channel number and time stamp. A programming interface accepts commands and data from a serial input bus and programmable registers are used to hold input values for DACs that provide currents and voltages required by the core, such as the threshold level for the discriminators and the amplitude of the test signal generated by an internal pulser. The data output interface accepts data from the core, serializes the data and transmits them off chip on as many as 6 output LVDS lines, with a maximum data transmission rate of 840 Mb/s. The number of output lines is programmable, depending on the expected hit activity in the chip. The size of the strip sets was chosen in order for the readout architecture to handle a 2 % average strip signal occupancy at a bunch crossing period of 132 ns, with an efficiency greater than 99 %.

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As far as analog performances are concerned, the analog channels were designed to achieve an Equivalent Noise Charge (ENC) smaller than 1000 e rms with a 20 pF detector capacitance  $C_D$  and a threshold dispersion across the chip smaller than 500 e rms. This allows for a low noise hit rate at a 0.2 MIP (Minimum Ionizing Particle) threshold setting.

Even if in an experiment like BTeV a simple binary output (Hit/No Hit) from each channel is sufficient for track reconstruction, in FSSR2 it was decided to include a low resolution ADC to calibrate the detector as radiation changes its characteristics.

The BTeV experiment set the requirement that the chip has to maintain its performances up to 5 Mrad total dose of ionizing radiation. To this purpose, enclosed geometry NMOS are used in the chip [3]. Specially designed registers are used to mitigate single event upset (SEU) problems. A discussion of these registers and measurement of their cross section are given in [4]. Since FSSR2 is a mixed signal design with very low noise requirements, care was taken to minimize noise coupling from the digital section to the analog section of the chip, as discussed in [1]. To this purpose, all digital pads use low voltage differential signals (LVDS).

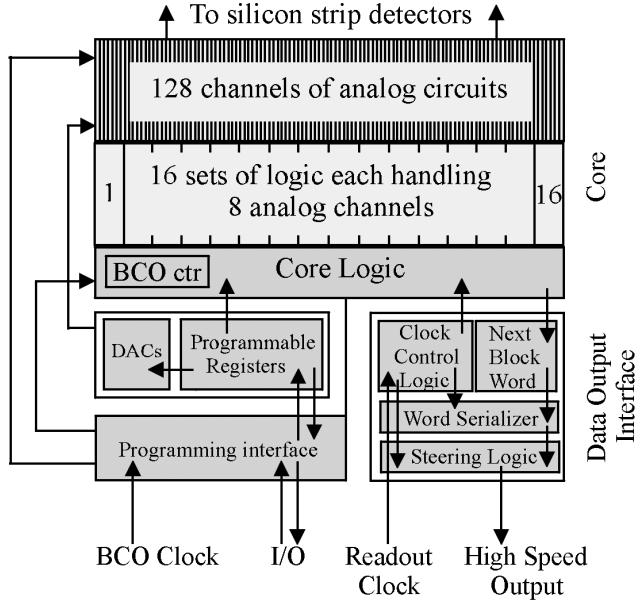


Fig. 2. Block diagram of the FSSR2 chip showing the core circuitry and the data output interface.

### B. Analog Section

The schematic diagram of the analog channel in FSSR2 is shown in Fig. 3. The front-end stage consists of a charge-sensitive preamplifier, followed by a unipolar second order semigaussian shaper. In the preamplifier, a continuous reset is provided by a transconductor (with transconductance  $G_f$ ). The shaping actually takes place in two steps. First the signal from the preamplifier undergoes an integration, then the shaping is completed by an active filter which provides one more

integration and a differentiation and also implements a gain function. The signal peaking time  $t_p$  at the shaper output is selectable among four values (65 ns, 85 ns, 100 ns, 125 ns) by acting on capacitor values in the shaper [5]. This allows for good operation with different hit rates in the detector.

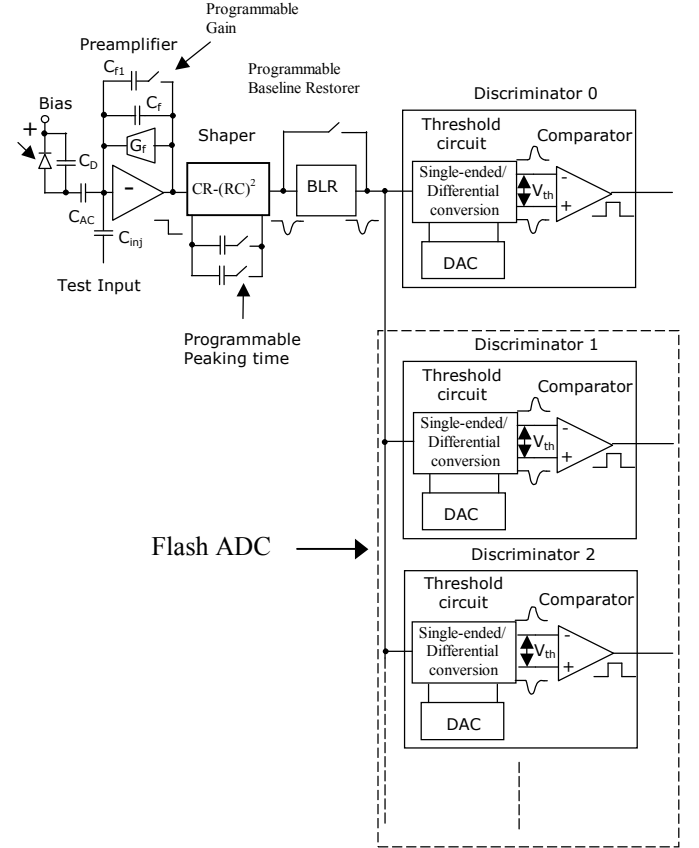


Fig. 3. Schematic of the analog channel in the FSSR2 chip. The DACs are shared by all 128 channels in the chip.

In the FSSR2, in the 128 channels the preamplifier input device is an NMOS with  $W/L = 1500/0.45$  biased at a drain current  $I_D = 500 \mu A$ . The choice of the input device was made on the basis of noise measurements on the prototype, showing that the NMOS is preferable to the PMOS because of its smaller white noise contribution in the relevant peaking time range. The gate width and length were chosen to attain the best performances for detector capacitances in the range from 10 to 30 pF [6], [7]. Noise measurements on single test devices included in the prototype FSSR chip yielded the results shown in Fig. 4. The plot compares the noise voltage spectra of an NMOS with the same gate dimensions chosen as the preamplifier input device in FSSR2 and of a PMOS with a similar  $W/L$  ratio. The normalized transfer function of the semigaussian shaper in FSSR2 is superimposed to the plot to highlight the frequency region of interest at different peaking time settings. The plot shows that the peaks of the transfer functions always occur where white noise is dominant, giving a clear advantage to the NMOS. As shown by Fig. 5, this conclusion was confirmed by ENC measurements on analog

channels integrated in the FSSR prototype, where the preamplifier input devices had the same gate dimensions as the NMOS and PMOS in Fig. 4.

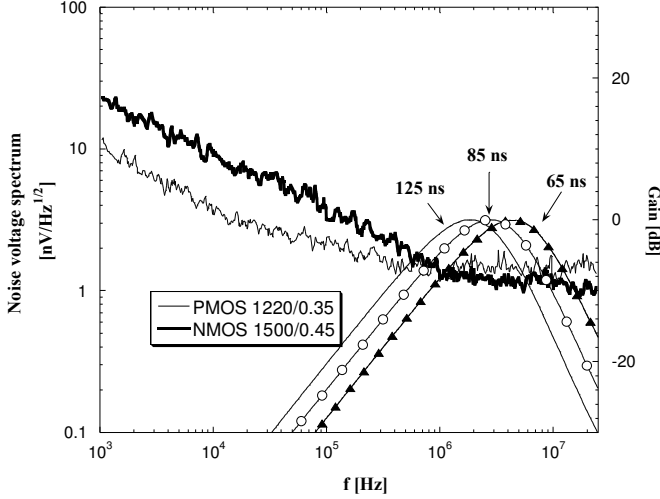


Fig. 4. Noise voltage spectra of a PMOSFET with  $W/L = 1220/0.35$  and an NMOSFET with  $W/L = 1500/0.45$  in the  $0.25 \mu\text{m}$  process by TSMC at  $I_D = 500 \mu\text{A}$ . The normalized transfer function of the semigaussian shaper in FSSR2 is superimposed to highlight the frequency regions of interest at three peaking time settings from  $t_p = 65 \text{ ns}$  to  $t_p = 125 \text{ ns}$ .

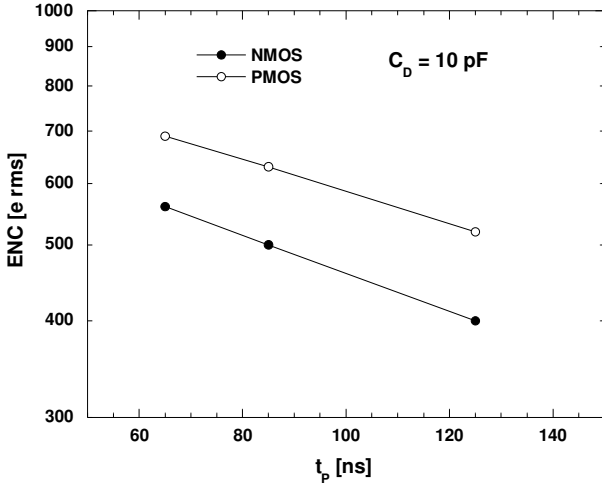


Fig. 5. Equivalent noise charge ENC as a function of the peaking time  $t_p$  at a detector capacitance  $C_D = 10 \text{ pF}$  for analog channels in the FSSR prototype. The plot reports values measured on channels with an NMOS ( $W/L = 1500/0.45$ ) and a PMOS ( $W/L = 1220/0.35$ ) at the preamplifier input, both biased at  $I_D = 500 \mu\text{A}$ . Data are relevant to channels that did not include a baseline restorer.

Several changes were made in the design of FSSR2 with respect to the prototype FSSR. First of all, the overall charge sensitivity  $G_Q$  was increased to reduce the discriminator threshold dispersion and meet the specifications with a good safety margin. Two nominal values of  $G_Q$  are selectable in FSSR2,  $150 \text{ mV/fC}$  and  $100 \text{ mV/fC}$ . The selection is achieved by acting on the preamplifier feedback capacitance, which can be increased from  $100 \text{ fF}$  to  $150 \text{ fF}$  (connecting the capacitor  $C_{f1}$  in parallel to  $C_f$ ) to reduce the gain and increase the linear

dynamic range. Secondly, after the shaper a baseline restorer can be used to cancel baseline shifts at the shaper output which affect the discriminator threshold. As shown in [1], a symmetric BLR is implemented according to the principles discussed in [8]. In FSSR2, the BLR is implemented in all channels in a programmable way, so that it may be used only when the strip signal occupancy is high. Limitations and advantages related to the BLR will be discussed in Section III. Finally, whereas the prototype FSSR provided only binary information concerning strip hits, in FSSR2 a 3-bit Flash ADC is implemented in each channel, giving analog information which may be used for detector monitoring and calibration. The discriminators in the ADC are driven by a threshold circuit, which converts the single-ended signal at the shaper output to a differential signal and superimposes a differential dc threshold voltage to the dynamic signal. A differential threshold voltage is used out of concern with crosstalk from the digital section on a single-ended threshold line. There is no threshold adjustment at the channel level: for all channels, the thresholds of the discriminators are set by DACs located in the programming interface. As shown by Fig. 3, discriminator 0 gives the binary information (Hit/NoHit). If it detects a hit, the 3 bit pulse amplitude information (generated by discriminators 1 to 7) for the relevant channel is attached to the output data word, as discussed in Section II-C. In FSSR2, 8-bit internal DACs are included to control critical reference voltages, discriminator thresholds and the amplitude of a calibration signal which can be injected by an internal pulser at the input of the analog channels. Outputs from any or all channels can be killed upon command from a dedicated register.

### C. Digital Section

A general description of the digital section and of the output data format is given in [1] for the FSSR prototype chip and will not be repeated here. In FSSR2, a few changes were made. Several DACs were added in the Programming Interface to provide various control functions, as discussed in Section II-B. The 24 bit output data word includes the 3 bits for the ADC pulse amplitude information. The other bits are used as follows: 8 bits for the BCO (Beam Crossing Oscillator) number associated with the hit, 5 bits for the number of the logic set handling the hit, 4 bits for the number of the hit silicon strip, and 1 bit for a word mark (3 bits are unused).

## III. CHIP PERFORMANCES

The FSSR2 chip has been successfully tested. Both the analog and digital sections have functioned properly, allowing extensive testing of the chip to be completed. In nominal operating conditions, for FSSR2 the power dissipation (including analog and digital sections) is about  $4 \text{ mW/channel}$ . The measurement of the critical parameters such as threshold dispersion and ENC was performed by detecting the firing efficiency of the Hit/NoHit discriminator with the threshold scan technique.

### A. Charge Sensitivity and Threshold Dispersion

As previously discussed the analog channel can operate in four different peaking time settings, selected by changing capacitor values in the shaper, and in two different gain settings, which are selected by acting on the preamplifier feedback capacitance. Fig. 6 shows measured waveforms at the shaper output at the four  $t_p$  settings, in the low gain condition. The charge sensitivity  $G_Q$  at the shaper output is about 120 mV/fC in this condition and is increased up to about 160 mV/fC in the high gain setting, as shown by Fig. 7. This plot compares the measured waveforms at the shaper and BLR outputs, showing the cancellation of the signal tail performed by the BLR. When the BLR is included,  $G_Q$  is reduced by about 20%.

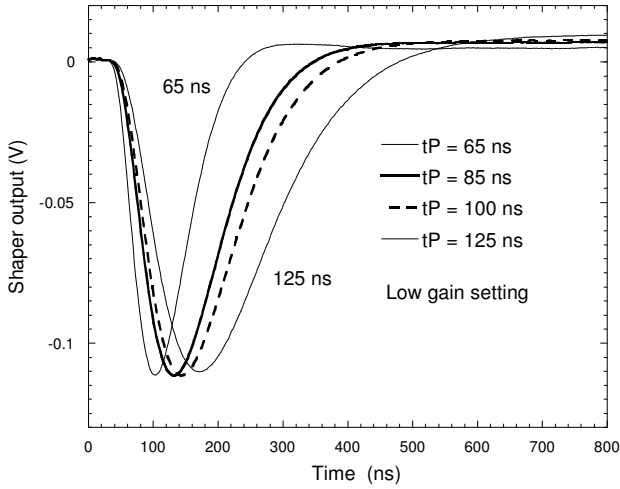


Fig. 6. Averaged waveforms at the shaper output of FSSR2 at different peaking time settings for 1 fC input charge.

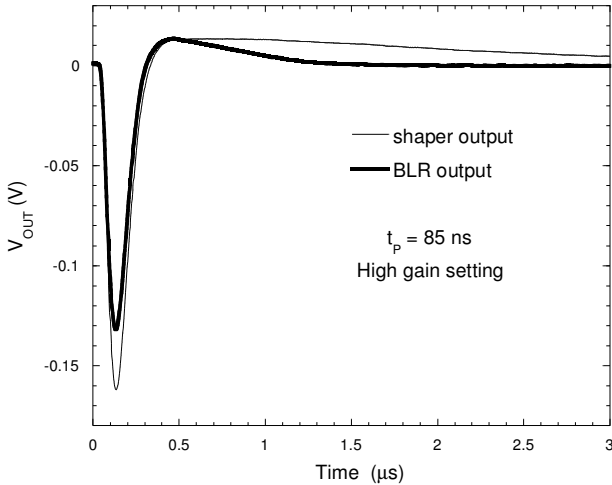


Fig. 7. Averaged waveforms at the output of the shaper and of the BLR at  $t_p = 85$  ns for 1 fC input charge.

Table I shows the measured values of the discriminator threshold dispersion  $\sigma_{Qth}$  expressed in terms of an input charge by dividing the comparator threshold voltage dispersion by the channel charge sensitivity  $G_Q$ . Since the main sources of

threshold dispersion are device mismatches in source-coupled pairs in the shaper, BLR and discriminator, an increase of the charge sensitivity brings along a reduction of  $\sigma_{Qth}$ . The results displayed in Table I show that the presence of the BLR reduces the threshold dispersion. Since the BLR is ac coupled to the shaper output, contributions to threshold dispersion coming from the previous blocks are suppressed when the BLR is selected. As also discussed in [1], the BLR used in FSSR and FSSR2 is effective in removing the threshold shift due to baseline fluctuations of the signal at the shaper output.

Table I shows that the specification  $\sigma_{Qth} < 500$  e rms is always met in the high gain condition, whereas, at low gain, the BLR has to be selected.

Fig. 8 shows the typical response of the ADC to different signal charges. The ADC range was centered around 1 MIP.

TABLE I  
TYPICAL THRESHOLD DISPERSION FOR CHANNELS WITH AND WITHOUT A BASE LINE RESTORER CIRCUIT FOR DIFFERENT GAIN AND PEAKING TIME SETTINGS

	Peaking time [ns]	Threshold dispersion [e rms]	
		Low Gain	High Gain
Channels with BLR deselected	65	580	460
	85	600	470
	125	615	485
Channels with BLR selected	65	440	295
	85	440	290
	125	490	280

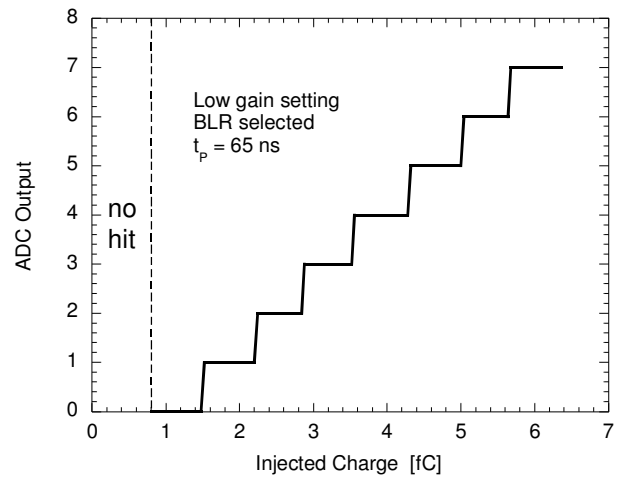


Fig. 8. Measured ADC response in FSSR2. The Hit/NoHit threshold was set at 0.8 fC. The ADC output is expressed in decimal format.

### B. Noise

Figs. 9 and 10 show the typical ENC values measured for the FSSR2 chip at different peaking time settings. Comparing the two plots, it can be noticed that ENC increases by about 15 % when the BLR is selected. This is in agreement with the expected behavior of a symmetric BLR as that used in FSSR2 [9]. However, the specification  $\text{ENC} < 1000 \text{ e rms}$  at  $C_D = 20 \text{ pF}$  is met with a good margin, except at  $t_p = 65 \text{ ns}$  with BLR selected, where ENC is just below  $1000 \text{ e rms}$ .

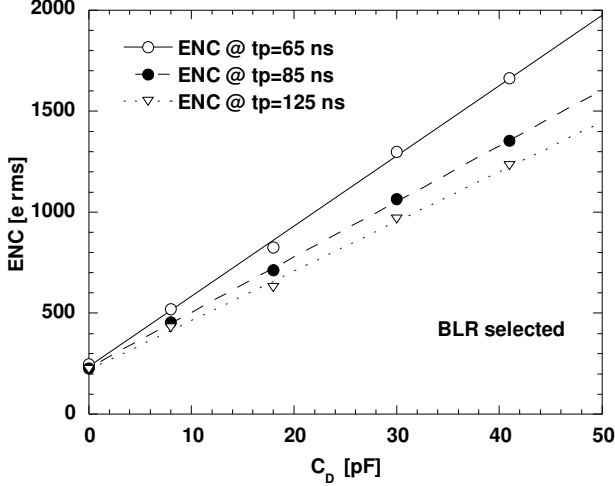


Fig. 9. Equivalent noise charge for a channel with baseline restorer at three peaking time settings as a function of the detector capacitance  $C_D$ .

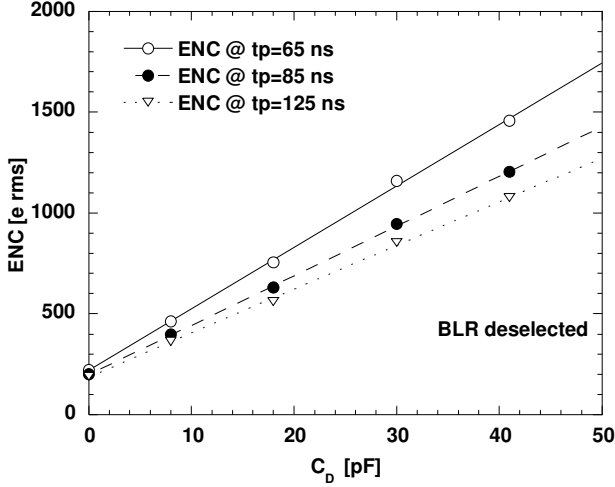


Fig. 10. Equivalent noise charge for a channel with baseline restorer deselected at three peaking time settings as a function of the detector capacitance  $C_D$ .

Table II reports the values of the ENC sensitivity to the detector capacitance  $d\text{ENC}/dC_D$  at different peaking time settings. Very little variations in ENC are observed if the gain setting is changed.

TABLE II  
TYPICAL EQUIVALENT NOISE CHARGE FOR CHANNELS WITH AND WITHOUT A BASE LINE RESTORER CIRCUIT FOR DIFFERENT PEAKING TIME SETTINGS

Channels with BLR selected			
Peaking time [ns]	65	85	125
ENC at $C_D = 0$ [e rms]	240	230	220
$d\text{ENC}/dC_D$ [e/pF]	35	28	24
Channels with BLR deselected			
Peaking time [ns]	65	85	125
ENC at $C_D = 0$ [e rms]	220	200	190
$d\text{ENC}/dC_D$ [e/pF]	31	25	21.5

### C. Radiation Tolerance

Different radiation hardness tests were performed on the FSSR prototype and on the FSSR2 chip. Since the chips are fabricated in the same technology and are based on very similar schematics, both using enclosed NMOSFETs, it can be reasonably assumed that the results of FSSR irradiation tests give valuable information about the behavior of FSSR2.

At the SIRAD facility located at the INFN Legnaro National Laboratory [10], the FSSR prototype was exposed to a  $1.9 \times 10^{13} \text{ cm}^{-2}$  fluence of 27 MeV protons, corresponding to a total ionizing dose of 5 Mrad, that is, the worst case expected for a 10 year operation in BTeV. The proton flux was about  $5.5 \times 10^9 \text{ cm}^{-2} \text{ s}^{-1}$ . The chips were irradiated with no bias applied. After irradiation the chip remains fully functional with very little ( $< 10 \%$ ) degradation of critical parameters such as ENC and threshold dispersion [11]. Fig. 11 compares the signal at the shaper output of a channel from a nonirradiated chip and channel from an irradiated FSSR. Only a slight difference is detected and it is hard to tell whether it should be ascribed to radiation effects or to chip-to-chip variations.

Some samples of the FSSR2 chip were exposed to  $\gamma$ -rays from a  $^{60}\text{Co}$  source with a dose rate of about  $16 \text{ rad}(\text{SiO}_2)/\text{s}$ . No bias was applied during irradiation. The circuits were exposed to a total ionizing dose of 19.4 Mrad, which is compatible with the radiation environment of LHC experiments. Measurements performed after irradiation show that  $\gamma$ -rays do not seem to affect noise and charge sensitivity. The variation of these parameters before and after irradiation are inside experimental errors and chip-to-chip variations ( $< 5 \%$ ). A larger effect is instead detected in the threshold dispersion when the BLR is selected, as shown by Table III.  $\sigma_{\text{Qth}}$  increases by about 15 %, but remains well below the required value of 500 e rms. The increase is smaller if the BLR is not used.

As a general remark, these irradiation tests confirm the high degree of ionizing radiation tolerance that can be achieved in the 0.25  $\mu\text{m}$  CMOS generation.

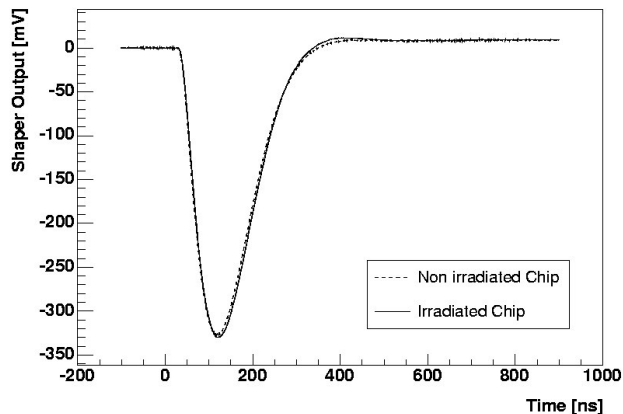


Fig. 10. Waveforms at the shaper output of channels in a non-irradiated FSSR chip and in an FSSR chip exposed to 27 MeV protons at a 4 fC input charge and peaking time setting  $t_p = 85$  ns.

TABLE III  
TYPICAL THRESHOLD DISPERSION BEFORE AND AFTER EXPOSURE TO 19.4 MRAD TOTAL DOSE OF  $\gamma$ -RAYS IN THE HIGH GAIN SETTING

	Peaking time [ns]	Non irradiated chip	Irradiated chip
	65	295 e rms	335 e rms
BLR selected	85	290 e rms	330 e rms
	125	280 e rms	320 e rms
BLR deselected	125	485 e rms	495 e rms

#### IV. CONCLUSION

The 128-channel chip FSSR2 was designed and successfully tested. The device is fully functional and meets demanding specifications in terms of noise and threshold dispersion. Because of its low noise, radiation tolerance and high data output bandwidth and of the flexibility provided by the various programmable features, FSSR2 can operate in different experimental environments and applications. Presently, FSSR2 is being evaluated in view of its possible operation in detector readout in a tracking system providing information to a first level trigger for both fixed target and collider experiments.

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#### REFERENCES

- [1] R. Yarema, J. Hoff, A. Mekkaoui, M. Manghisoni, V. Re, P. F. Manfredi, L. Ratti, V. Spezioli, "Fermilab Silicon Strip Readout Chip for BTeV", *IEEE Trans. Nucl. Sci.*, vol. 52, No. 3, pp. 799-804, 2005.
- [2] D.C. Christian, J.A. Appel, G. Cancelo, J. Hoff, S. Kwan, A. Mekkaoui, R. Yarema, et al. "FPIX2: a radiation-hard pixel readout chip for BTeV", *Nucl. Instr. Meth.*, vol. A473, pp. 152-156, 2001.
- [3] G. Anelli, M. Campbell, M. Delmastro, F. Faccio, S. Florian, et al., "Radiation Tolerant VLSI Circuits in Standard Deep Submicron CMOS Technologies for the LHC Experiments: Practical Design Aspects," *IEEE Trans. Nucl. Sci.*, vol. 46, no. 6, pp. 1690-1695, Dec. 1997.
- [4] G. Chiodini, J. A. Apple, G. Cardoso, D. C. Christian, M. R. Coluccia, J. Hoff, S. W. Kwan, A. Mekkaoui, R. Yarema, and S. Zimmermann, "Radiation Tolerance Studies of BTeV Pixel Readout Chip Prototypes", presented at the 7th Workshop on Electronics for LHC Experiments, Stockholm Sweden, September 10-14, 2001, published in *Stockholm 2001, Electronics for LHC Experiments*, pp 67-70.
- [5] P.F. Manfredi, I. Kipnis, E. Mandelli, V. Re, N. Roe, et al., "The analog front-end section of the BaBar silicon vertex tracker readout IC", *Nuclear Physics B (Proc. Suppl.)* 61B (1998) pp. 532-538.
- [6] V. Re, L. Ratti, M. Manghisoni, V. Spezioli, G. Traversi, "Survey of Noise Performances and Scaling Effects in Deep Submicron CMOS Devices from Different Foundries", presented at 2004 IEEE Nuclear Science Symposium, Rome, Italy, October 16-22, 2004.
- [7] M. Manghisoni, L. Ratti, V. Re, V. Spezioli, "Submicron CMOS technologies for low-noise analog front-end circuits", *IEEE Trans. Nucl. Sci.*, vol. 49, No. 4, pp. 1783-1790, 2002.
- [8] R. L. Chase and L. R. Poulou, "A high precision DC restorer", *IEEE Trans. Nucl. Sci.*, vol. 14, no. 6, pp. 83-87, Dec. 1967.
- [9] V. Radeka, "The effect of baseline restoration on signal-to-noise ratio in pulse amplitude measurements," *Rev. Sci. Instr.*, vol. 38, 1967, p. 1397.
- [10] J. Wyss, D. Bisello, and D. Pantano, "SIRAD: an irradiation facility at the LNL Tandem accelerator for radiation damage studies on semiconductor detectors and electronic devices and systems", *Nucl. Instr. Meth.*, vol. A462, pp. 426-434, 2001.
- [11] L. Ratti, M. Manghisoni, V. Re, G. Traversi, and A. Candelori, "Radiation hardness test of FSSR, a multichannel, mixed signal chip for microstrip detector readout", presented to the 8th European Conference on Radiation and Its Effects on Components and Systems (RADECS 2005), Cap D'Agde, France, September 19-23, 2005.